



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/656,165	09/08/2003	Sungkwon Chris Hong	M4065.0916/P916	1326

24998 7590 04/17/2006

DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street, NW
Washington, DC 20037

EXAMINER

YAM, STEPHEN K

ART UNIT	PAPER NUMBER
----------	--------------

2878

DATE MAILED: 04/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

2

Office Action Summary

Application No.

10/656,165

Applicant(s)

HONG ET AL.

Examiner

Stephen Yam

Art Unit

2878

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 January 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-4 and 6-46 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 4, 6-14, 16-28, 31-36, 38-42, 44 and 46 is/are rejected.
- 7) ☒ Claim(s) 2, 3, 15, 29, 30, 37, 43 and 45 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This action is in response to Amendments and remarks filed on January 13, 2006. Claims 1-4 and 6-46 are currently pending.

Claim Objections

1. Claim 40 is objected to because of the following informalities:

In Claim 40, "said *second* polysilicon layer" lacks proper antecedent basis.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Kwon US Patent No. 6,809,309.

Regarding Claim 1, Kwon teaches (see Fig. 4A and 6) a pixel sensor cell comprising a substrate (61, 62), a photoelectric conversion device (46/ 63,64) comprising a region (64) of a first conductivity type (p-type) at a surface of the substrate (see Fig. 6) and a region (63) of a second conductivity type (n-type) below the first conductivity type region, a gate (68) located over said photoconversion device (see Fig. 6), a contact (attached to Px- see Fig. 4A) connected

Art Unit: 2878

to said gate, a charge collection region (42/67) for receiving charges from said photoconversion device (see Col. 4, lines 19-24 and Col. 5, lines 24-27, 55-58), and a transistor (45/65) (see Fig. 4A and 6) for transferring charge from said photoconversion device to said charge collection region (see Col. 4, lines 11-14 and Col. 5, lines 55-58).

Regarding Claim 7, Kwon teaches the charge collection region comprising a floating diffusion region (see Col. 5, lines 24-27).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 20, 22-24, 26, 27, 44, and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon.

Regarding Claim 20, Kwon teaches (see Fig. 4A, 5, 6) an imager (see Col. 3, lines 63-67) comprising an array of pixel sensor cells (see Col. 3, lines 63-67), each pixel sensor cell having a photoconversion device (46/ 63,64), a substrate (61, 62) having a first surface level (top surface of (62)), said photoconversion devices being located within said substrate (see Fig. 6) and comprising a region (64) of a first conductivity type (p-type) at a surface of the substrate (see Fig. 6) and a region (63) of a second conductivity type (n-type) below the first conductivity type region, photodiode gates (68) located over said substrate first surface level and over said photoconversion devices (see Fig. 6), and contacts (attached to Px- see Fig. 4A) connected to

Art Unit: 2878

said photodiode gates, and signal processing circuitry (43) and electrically connected to the array for receiving and processing signals representing an image output by the array and for providing output data representing said image. Kwon does not teach the signal processing circuitry formed in the substrate. It is well known in the art to form transistor components within the semiconductor substrate, to provide integration and improved electrical effects. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the signal processing circuitry formed in the substrate, in the imager of Kwon, to provide improved transistor integration with the substrate and reduce electrical noise.

Regarding Claim 24, Kwon teaches (see Fig. 4A, 5, 6) a system comprising a substrate (61, 62) having a first surface level (top surface of (62)), a photoconversion device (46/ 63,64) located within said substrate (see Fig. 6) and comprising a region (64) of a first conductivity type (p-type) at a surface of the substrate (see Fig. 6) and a region (63) of a second conductivity type (n-type) below the first conductivity type region, a photodiode gate (68) located over said substrate first surface level and over said photoconversion devices (see Fig. 6), and a contact (attached to Px- see Fig. 4A) connected to said photodiode gate, and a readout circuit (44) (see Fig. 4A) comprising at least an output transistor formed on said substrate (since the image sensor is formed on a single chip- see Col. 1, lines 21-24). Kwon does not teach the system comprising a processor. It is well known in the art to provide an image processor in an image sensor system, to process the sensor output for optimizing the image for color, contrast, clarity, etc. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a processor in the system of Kwon, to improve the image output for optimal imaging.

Regarding Claims 22 and 26, Kwon teaches the pixel sensor cell as part of a CMOS imager (see Col. 3, lines 63-67).

Regarding Claims 23 and 27, Kwon teaches the system in Claims 20 and 24, according to the appropriate paragraph above. Kwon does not teach the sensor as part of a charge coupled device (CCD) imager. It is well known in the art to select between configuring an image sensor as CCD or CMOS and that a CCD imager provides greater light sensitivity for imaging. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the sensor as part of a CCD imager in the system of Kwon, to provide improved detection sensitivity for improved low-light detection.

Regarding Claims 44 and 46, Kwon teaches the gate reducing an energy barrier between said photoconversion device and said charge collection region (see Col. 4, lines 49-54).

6. Claims 4, 8-14, 16-19, 21, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon in view of Ohmi et al. US Patent No. 5,128,735.

Regarding Claims 4, 8, 17, 21, and 25, Kwon teaches the device and elements of Claims 1, 20, and 24, according to the appropriate paragraph above. Regarding Claim 8, Kwon also teaches the substrate having a first surface level (top surface of (62)- see Fig. 6), the first and second regions as doped (see Col. 5, lines 12-18), and the transistor located adjacent to said photoconversion device (see Fig. 6). Kwon also teaches the gate formed over the first surface level of the substrate to form a second surface level (see Fig. 6) and comprising a dielectric substance layer (since the gate has capacitance/charge storage effects- see Fig. 4A). Kwon does not teach the gate comprising a polysilicon layer with the contact connected to the polysilicon

Art Unit: 2878

layer, or the polysilicon layer overlapping at least a portion of the transistor. Ohmi et al. teach (see Fig. 21a, 21b) a similar device with a photodiode gate (271) located above a substrate first surface level and over a photoconversion device (see Fig. 21a), with the photodiode gate having a polysilicon layer (see Col. 41, lines 11-13) and a contact (274) connected to the polysilicon layer (see Fig. 21b) with a transistor (273, 270, 7) and the polysilicon layer overlapping at least a portion (270, 7) of the transistor. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the gate comprising a polysilicon layer with the contact connected to the polysilicon layer with the polysilicon layer overlapping at least a portion of the transistor, as taught by Ohmi et al., in the device of Kwon, to improve the electrical characteristics of the gate for improved transistor function.

Regarding Claim 16, Kwon teaches the transistor comprising a transfer transistor (see Fig. 4A and Col. 4, lines 11-14).

Regarding Claim 18, Kwon teaches the pixel sensor cell as part of a CMOS imager (see Col. 3, lines 63-67).

Regarding Claims 9 and 13, Kwon in view of Ohmi et al. teach the device in Claim 8, according to the appropriate paragraph above. Kwon does not teach the dielectric substance layer having a thickness in the range of about 50-150 Å or the polysilicon layer having a thickness in the range of 500-1500 Å. It is well known in the art to select appropriate thicknesses for layers within a semiconductor system, depending on the desired operating conditions of each layer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the claimed layer thicknesses, for the device of Kwon in view of Ohmi et al., since it has been held that where the general conditions of a claim are

Art Unit: 2878

disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Regarding Claims 10-12 and 14, Kwon in view of Ohmi et al. teach the device in Claim 8, according to the appropriate paragraph above. Kwon does not teach the dielectric substance layer comprising silicon dioxide, silicon nitride, or silicon oxynitride, or the polysilicon layer comprising silicon germanium. It is well known in the art to determine and select appropriate compounds for constructing a layer within a semiconductor system, and that silicon dioxide, silicon nitride, silicon oxynitride, and silicon germanium are common semiconductor materials. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide to use silicon dioxide, silicon nitride, silicon oxynitride, and silicon germanium for the layers, in the device of Kwon in view of Ohmi et al., since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Regarding Claim 19, Kwon in view of Ohmi et al. teach the device in Claim 8, according to the appropriate paragraph above. Kwon does not teach the sensor as part of a charge coupled device (CCD) imager. It is well known in the art to select between configuring an image sensor as CCD or CMOS and that a CCD imager provides greater light sensitivity for imaging. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the sensor as part of a CCD imager in the device of Kwon in view of Ohmi et al., to provide improved detection sensitivity for improved low-light detection.

Art Unit: 2878

7. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon in view of Park US Patent No. 6,040,593.

Regarding Claim 6, Kwon teaches the device in Claim 1, according to the appropriate paragraph above. Kwon does not teach the photoconversion device comprising a pinned photodiode. Park teaches (see Fig. 3) a similar device, with a photoconversion device as a pinned photodiode (see Col. 3, line 67 to Col. 4, line 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the photoconversion device was a pinned photodiode, as taught by Park, in the device of Kwon, to provide appropriate operating characteristics for the photoconversion device for optimal light detection.

8. Claims 28, 31-36, and 38-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon in view of Park, further in view of Ohmi et al.

Regarding Claims 28 and 40, Kwon teaches (see Fig. 4A, 5, 6) a method of forming a sensor, comprising forming a substrate (61, 62) having a first surface level (top surface of (62)), forming a photoconversion device (46/ 63,64), said photoconversion device having a first doped region (64) of a first conductivity type (p-type) and a second doped region (63) of a second conductivity type (n-type) beneath said first surface level of said substrate (see Fig. 6), forming a photodiode gate (68) including a dielectric substance layer (since the gate has capacitance/charge storage effects- see Fig. 4A) over said first surface level of said substrate (see Fig. 6), thereby forming a second surface level (see Fig. 6), connecting a contact (Px) to said photodiode gate (see Fig. 4A and 6), and forming a charge collection region (42/67) for receiving charges from said photoconversion device (see Col. 4, lines 19-24 and Col. 5, lines 24-27, 55-58). Kwon does

Art Unit: 2878

not teach the photoconversion device with a pinning voltage or forming a polysilicon layer over said second surface level or the polysilicon layer overlapping at least a portion of the transistor. Park teaches (see Fig. 3) a similar device, with a photoconversion device with a pinning voltage (see Col. 3, line 67 to Col. 4, line 2). Kwon and Park do not teach forming a polysilicon layer over said second surface level or the polysilicon layer overlapping at least a portion of the transistor. Ohmi et al. teach (see Fig. 21a, 21b) a similar device with a photodiode gate (271) located above a substrate first surface level and over a photoconversion device (see Fig. 21a), with the photodiode gate having a polysilicon layer (see Col. 41, lines 11-13) and a contact (274) connected to the polysilicon layer (see Fig. 21b) with a transistor (273, 270, 7) and the polysilicon layer overlapping at least a portion (270, 7) of the transistor. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the gate comprising a top polysilicon layer with the contact connected to the polysilicon layer with the polysilicon layer overlapping at least a portion of the transistor, as taught by Ohmi et al., and to provide the photoconversion device with a pinning voltage, as taught by Park, in the device of Kwon, to improve the electrical characteristics of the gate for improved transistor function and to provide appropriate operating characteristics for the photoconversion device for optimal light detection.

Regarding Claims 31 and 35, Kwon in view of Park and Ohmi et al. teach the method in Claim 28, according to the appropriate paragraph above. Kwon does not teach the dielectric substance layer having a thickness in the range of about 50-150 Å or the polysilicon layer having a thickness in the range of 500-1500 Å. It is well known in the art to select appropriate thicknesses for layers within a semiconductor system, depending on the desired operating

conditions of each layer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the claimed layer thicknesses, for the method of Kwon in view of Park and Ohmi et al., since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Regarding Claims 32-34 and 36, Kwon in view of Park and Ohmi et al. teach the method in Claim 28, according to the appropriate paragraph above. Kwon does not teach the dielectric substance layer comprising silicon dioxide, silicon nitride, or silicon oxynitride, or the polysilicon layer comprising silicon germanium. It is well known in the art to determine and select appropriate compounds for constructing a layer within a semiconductor system, and that silicon dioxide, silicon nitride, silicon oxynitride, and silicon germanium are common semiconductor materials. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide to use silicon dioxide, silicon nitride, silicon oxynitride, and silicon germanium for the layers, in the method of Kwon in view of Park and Ohmi et al., since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Regarding Claim 38, Kwon teaches the charge collection region comprising a floating diffusion region (see Col. 5, lines 24-27).

Regarding Claim 39, Kwon teaches a transfer transistor (45/65) (see Fig. 4A and Col. 4, lines 11-14).

Art Unit: 2878

Regarding Claim 41, Kwon teaches said sensor as part of a CMOS imager (see Col. 3, lines 63-67).

Regarding Claim 42, Kwon in view of Park and Ohmi et al. teach the method in Claim 28, according to the appropriate paragraph above. Kwon does not teach the sensor as part of a charge coupled device (CCD) imager. It is well known in the art to select between configuring an image sensor as CCD or CMOS and that a CCD imager provides greater light sensitivity for imaging. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the sensor as part of a CCD imager in the method of Kwon in view of Park and Ohmi et al., to provide improved detection sensitivity for improved low-light detection.

Allowable Subject Matter

9. Claims 2, 3, 15, 29, 30, 37, 43, and 45 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding Claims 2, 29, 43, and 45, the invention as claimed, specifically in combination with the pixel sensor cell arranged such that the photoconversion device has a reduced pinning voltage V_{PIN} when a negative bias is applied to the contact, is not disclosed or made obvious by the prior art of record.

Regarding Claims 15 and 37, the invention as claimed, specifically in combination with a dielectric substance layer formed over the first surface level of the substrate thereby forming a second surface level, a polysilicon layer formed over said second surface level, wherein the

Art Unit: 2878

polysilicon layer comprises silicon germanium in a ratio of about $\text{Si}_{60}\text{Ge}_{40}$, is not disclosed or made obvious by the prior art of record.

Response to Arguments

10. Applicant's arguments with respect to claims 1-46 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen Yam whose telephone number is (571)272-2449. The examiner can normally be reached on Monday-Friday 8:30am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Georgia Epps can be reached on (571)272-2328. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SY

SY


THANH X. LUU
PRIMARY EXAMINER